Today, we can notice video capturing devices in numerous fields. For instance, defense and industrial technologies, quality control, product counting systems, services and so on. Due to technological developments, the quality of the captured videos is increased. To store these high-quality videos, video compression is compulsory. H.264 video compression standard uses various prediction modes to reduce the amount of data. The methods that are used and the data should be coded precisely to achieve high compression performance. For this purpose, H.264 presents Context Adaptive Binary Arithmetic Coding (CABAC) in high profile. CABAC includes three main modules which are binarization, context modeler and binary arithmetic coding engine. In this project, CABAC Encoder algorithm is analyzed from ITU-T/ISO/IEC standard document [1]. The MATLAB software model of the algorithm is developed for further verification purposes. Finally, as it can be seen from Figure 1, the first block of CABAC Encoder algorithm is implemented in VHDL. Binarizer hardware is verified using JM reference software and synthesized for Altera Cyclone V FPGA board with clock frequency of 200 MHz.

OBJECTIVES

• Literature review on CABAC Encoder Algorithm.
• Developed and verified MATLAB model of CABAC Encoder modules.
• Hardware implementation and analysis of Binarization and Context Modeler module in VHDL.
• Timing analysis and optimization using Quartus Prime tool.

CONCLUSION

Currently Binarization module is synthesized for Altera Cyclone V FPGA board. The module works with 200 MHz clock period and allocates 634 ALMs, 819 registers. Also, hardware implementation of Context Modeler is under development and it is planned be implemented before the final report.

REFERENCES
