H.264 CABAC Encoder Hardware Design and Implementation

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ABSTRACT

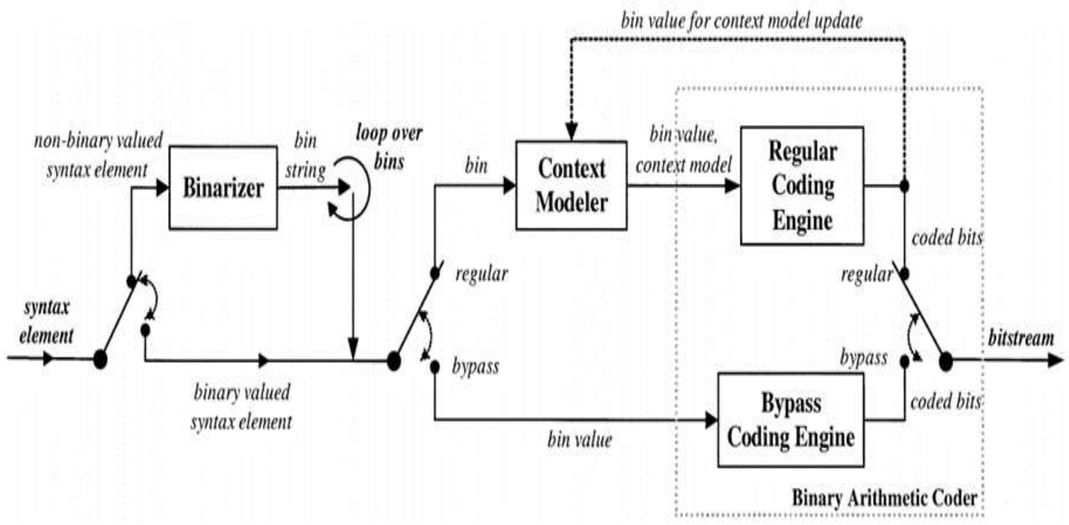

Figure – 1: CABAC Encoder Architecture [1]

Today, we can notice video capturing devices in numerous fields. For instance, defense and industrial technologies, quality control, product counting systems, services and so on. Due to technological developments, the quality of the captured videos is increased. To store these high-quality videos, video compression is compulsory. H.264 video compression standard uses various prediction modes to reduce the amount of data. The methods that are used and the data should be coded precisely to achieve high compression performance. For this purpose, H.264 presents Context Adaptive Binary Arithmetic Coding (CABAC) in high profile. CABAC includes three main modules which are binarization, context modeler and binary arithmetic coding engine. In this project, CABAC Encoder algorithm is analyzed from ITU-TE/ISO/IEC standard document [1]. The MATLAB software model of the algorithm is developed for further verification purposes. Finally, as it can be seen from Figure – 1, the first block of CABAC Encoder algorithm is implemented in VHDL. Binarizer hardware is verified using JM reference software and synthesized for Altera Cyclone V FPGA board with clock frequency of 200 MHz.

OBJECTIVES

- Literature review on CABAC Encoder Algorithm.
- Developed and verified MATLAB model of CABAC Encoder modules.
- Hardware implementation and verification of Binarization module in VHDL.
- Timing analysis and optimization using Quartus Prime tool.

CONTEXT MODELER & BINARY ARITHMETIC ENCODER

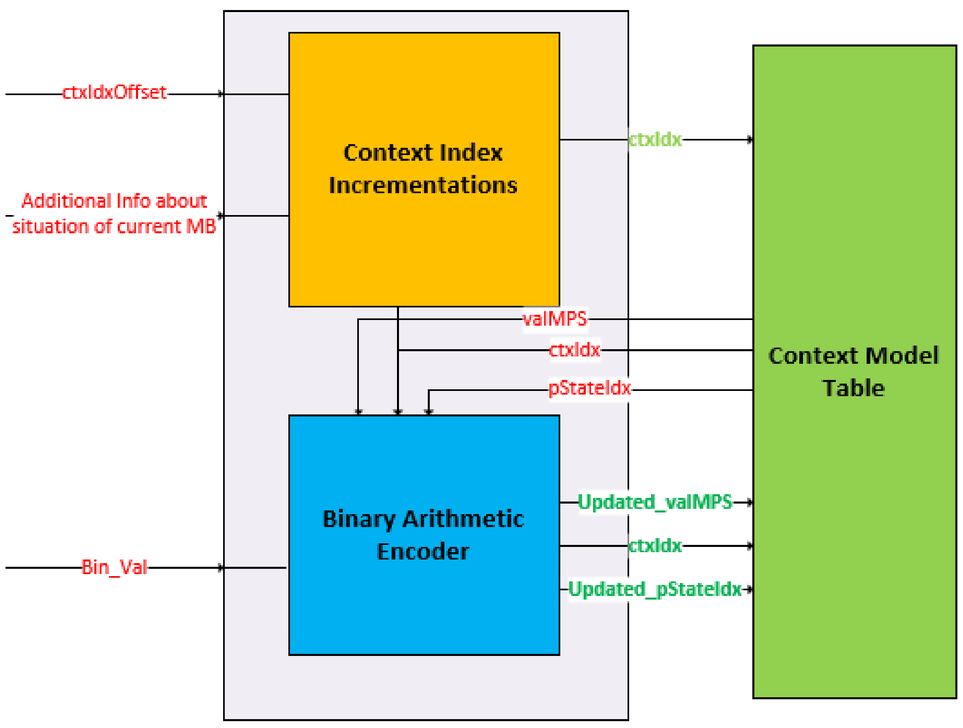

Figure – 2: Software Model of Context Modeler and Binary Arithmetic Encoder

H.264 video compression standard processes frames in 16x16 macroblocks. Each macroblock has several attributes and they are called ‘Syntax Element’ in the standard document. Binarization module takes value of each syntax element and uniquely maps them to bin strings. After Binarization, each bin is processed separately according to their context index numbers where these unique numbers is mapped to a probability state. According to the probability state and value of the most probable symbol, Binary Arithmetic Encoder encodes the given binary symbol.

HARDWARE IMPLEMENTATION OF BINARIZATION MODULE

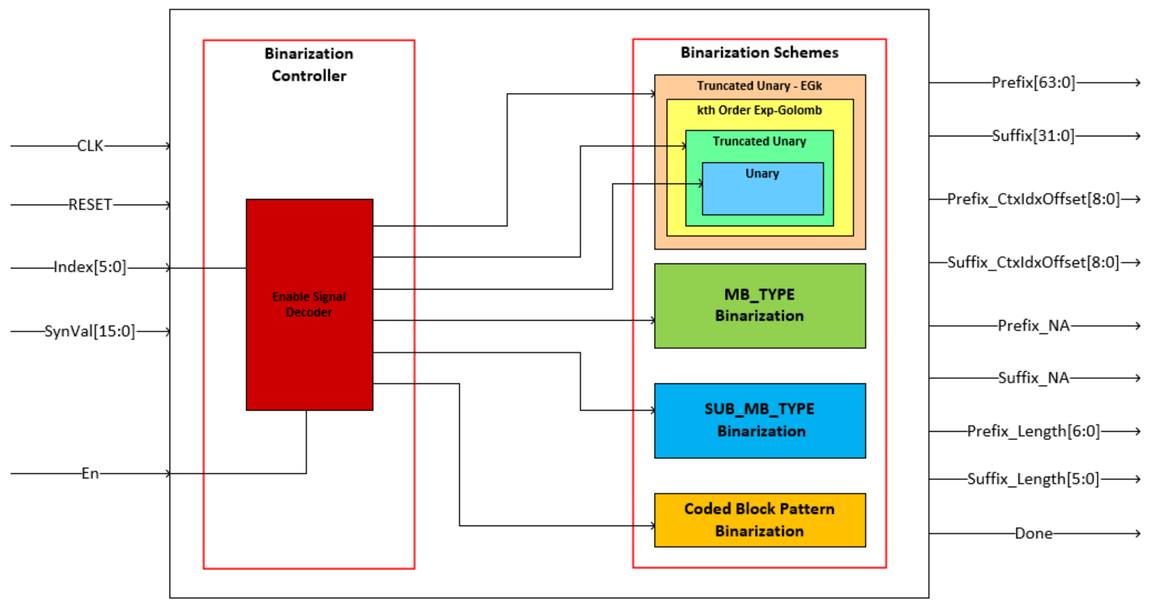

Figure – 3: Hardware Model of Binarization Module

Binarization operation contains several types of Binarization Schemes such as Unary, Truncated-Unary, Fixed-Length, Exp-Golomb. Also, in H.264 standard there are custom binarization schemes and concatenation of single binarization schemes. The custom binarization schemes are simply tables that maps a value to corresponding binarization.

Hardware implementation contains a controller which selects a binarization scheme that should be applied according to standard document. This selection is provided according to an ‘Index’ input where each index value represents a specific type of a syntax element. Application of binarization schemes varies according to slice type, macroblock type and value of the syntax element. After necessary binarization schemes is selected and applied controller provides the binarized bitstream and length of the bitstream. Outputs related to next module is also provided such as, ctxIdxOffset and maxBinIdxCtx.

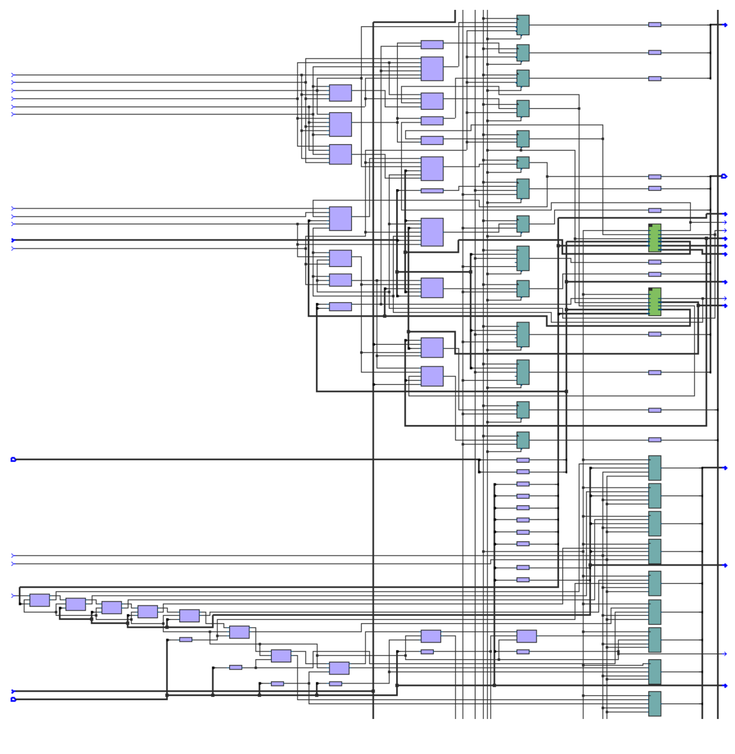

Figure – 4: Snapshot of synthesized Binarization module with Quartus Prime

CONCLUSIONS

Currently Binarization module is synthesized for Altera Cyclone V FPGA board. The module works with 200 MHz clock period and allocates 634 ALMs, 819 registers. Also, hardware implementation of Context Modeler is under development and it is planned be implemented before the final report.

REFERENCES

[1] *Information technology - Coding of audio-visual objects - Part 10: Advanced video coding=Technologies de linformation - Codage des objets audiovisuels - Partie 10: Codage visuelavance*. (2008). West Conshohocken, PA: International Organization for Standardization (ISO) and the International Electrotechnical Commission (IEC).

[2] Marpe, D., Schwarz, H., & Wiegand, T. (2003). Context-based adaptive binary arithmetic coding in the H.264/AVC video compression standard. IEEE Transactions on Circuits and Systems for Video Technology, 13(7), 620-636. doi:10.1109/tcsvt.2003.815173