Galileo GNSS RF Front End Receiver Design and Implementation

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ANKASYS

ABSTRACT

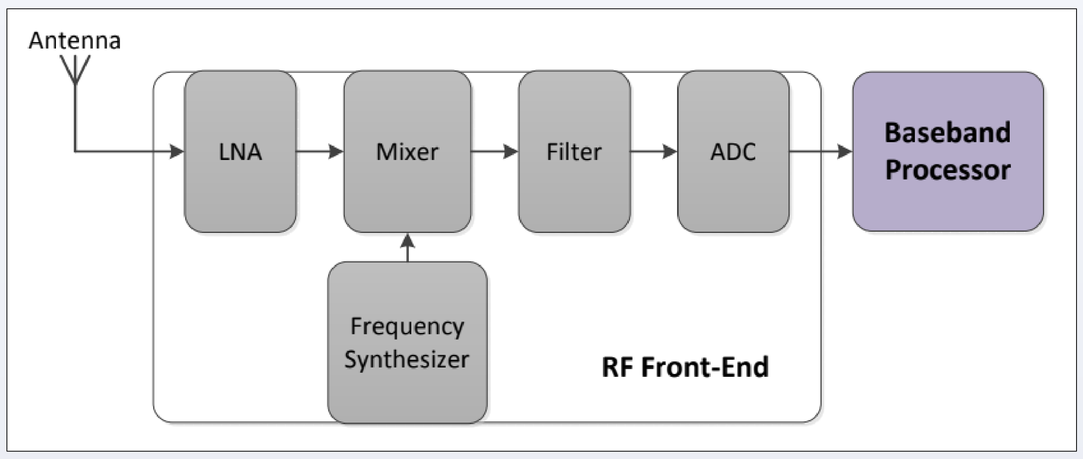

Figure 1. RF front-end architecture (main blocks). Adapted from [1]

This project presents the design of a single-ended cascode Low Noise Amplifier (LNA) for an RF front-end receiver for the Galileo E1 band at 1575.42 MHz, implemented using TSMC 65 nm CMOS technology. Based on a detailed review of academic and commercial GNSS front-end designs, the performance targets were set as a noise figure (NF) lower than 1 dB and a gain higher than 18 dB. The final design achieves a simulated NF of 0.99 dB and a gain of 19.78 dB. Reaching this level of performance required increased power consumption, reflecting the fundamental trade-off between noise reduction and power efficiency in RF design. In addition to its high gain and low noise characteristics, the amplifier exhibits wideband matching behavior even though this was not a primary goal, enhancing its suitability for integration into multi-band GNSS front-end systems.

OBJECTIVES

- Conduct an extensive literature review to analyze existing academic and commercial GNSS front-end solutions.
- Design a CMOS LNA for the Galileo E1 band at 1575.42 MHz using Advanced Design System (ADS).
- Achieve an NF lower than 1 dB and a gain higher than 18 dB.
- Optimize device sizing and biasing for simultaneous noise and power matching.
- Explore and evaluate trade-offs between key performance metrics such as gain, noise, and power.
- Develop an LNA design suitable for integration into a complete RF front-end system.

PROJECT DETAILS

While ANKASYS primarily focuses on the digital design aspects of GNSS receiver chips—such as baseband processing, digital correlators, and verification flows—it is also actively exploring the RF front-end domain to build broader design capabilities across the entire GNSS signal chain.

To this end, ANKASYS funded this project and established a collaborative research partnership with Sabancı University, leveraging academic expertise in analog/RF circuit design. The resulting LNA design for the Galileo E1 band represents an important milestone toward ANKASYS's long-term goal of offering end-to-end GNSS chip solutions, spanning both RF and digital domains.

Performance targets for the LNA were defined based on recent literature and commercial GNSS receivers. Academic works typically report noise figures in the range of 1.4–1.7 dB using similar CMOS technologies [2,3]. LNAs in the commercial products of Maxim Integrated demonstrate NF values as low as 0.9 dB, setting a high benchmark.

The design process began with a preliminary implementation using IHP SiGe technology, due to early access to its PDK. Once the feasibility of the topology was validated, the work transitioned to TSMC 65 nm CMOS, the intended fabrication process. Initial CMOS-based iterations used ideal passive components to speed up simulation and simplify parameter tuning. In later stages, realistic components from the TSMC PDK were adopted to capture parasitic effects and finalize the design.

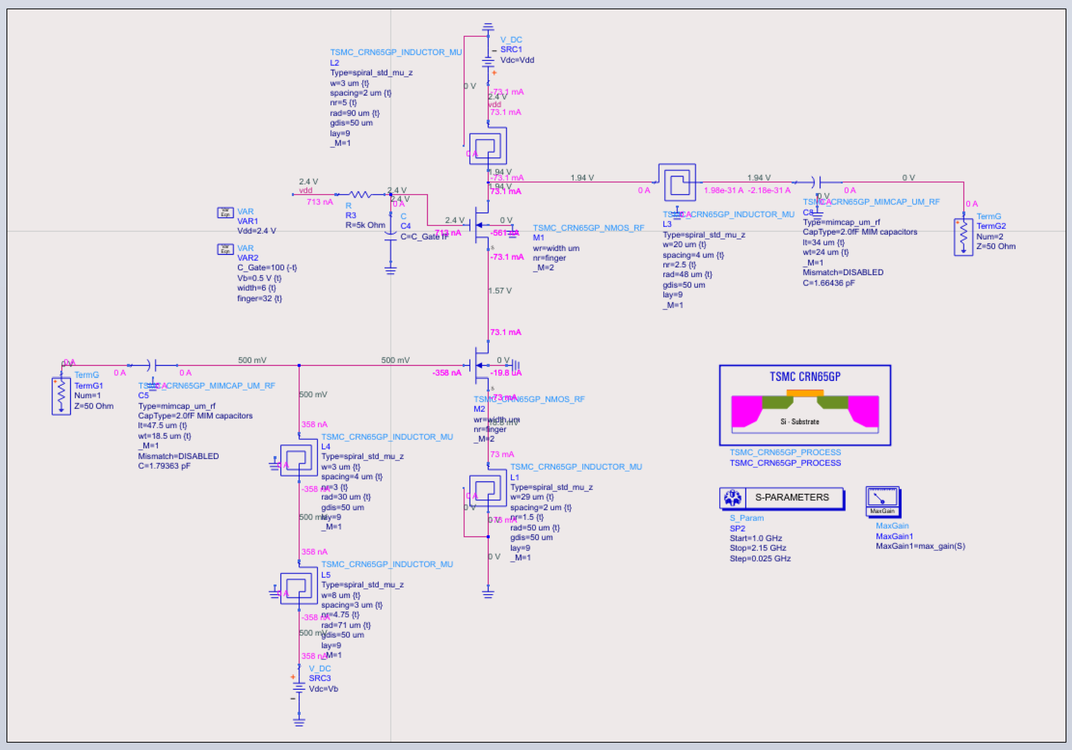

Figure 2. Schematic of the final LNA design

RESULTS

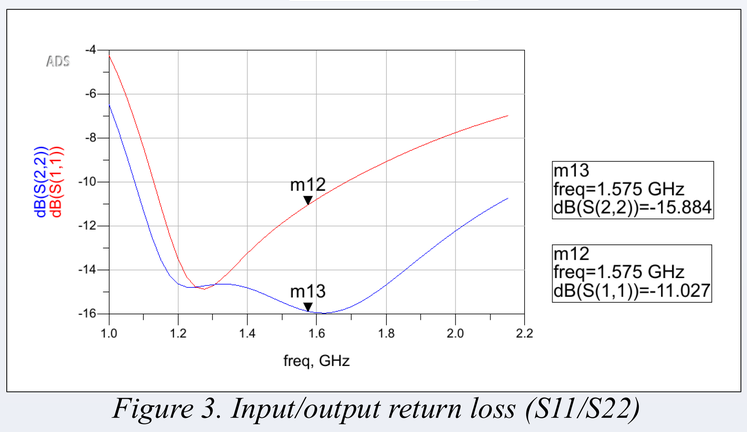

Figure 3. Input/output return loss (S11/S22)

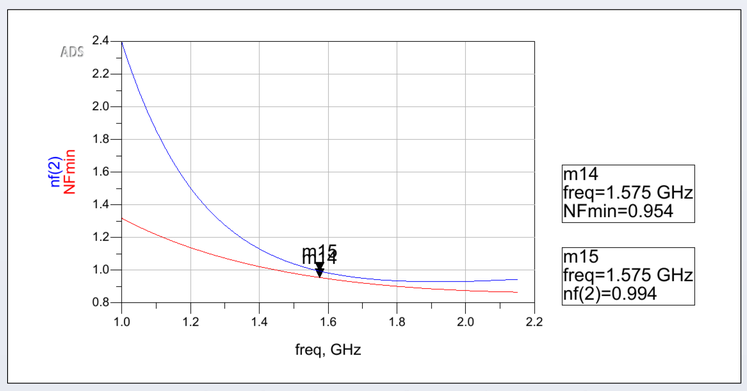

Figure 4. Simulated noise figure (NF) and NFmin

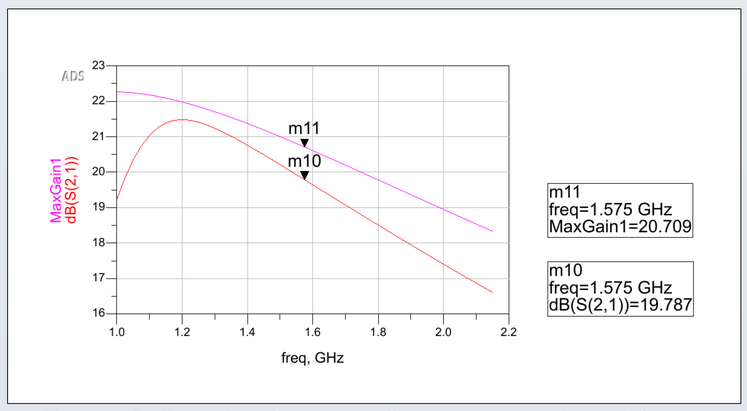

Figure 5. Simulated gain and maximum achievable gain

As shown in the figures, the amplifier achieves a gain of approximately 19.78 dB, satisfying the gain requirement. The simulated NF reaches 0.99 dB, which meets the design goal of sub-1 dB and confirms the effectiveness of transistor sizing, bias tuning, and noise matching strategies applied during optimization.

Input and output return losses are both below the -10 dB threshold, indicating sufficient matching and efficient power transfer. Although wideband operation was not explicitly targeted, the return loss behavior in Figure 3 indicates that wideband matching emerged as a byproduct of final tuning.

	This work	[2]	[3]	Maxim 2771
Technology	CMOS 65nm	CMOS 65nm	CMOS 65nm	not stated
Gain (dB)	19.78	18	18.5	18
NF (dB)	0.99	1.4	1.7	0.9
S11 (dB)	-11	~ -5	~ -8	-10
S22 (dB)	-15.9	~ -15	~ -12	-10
Power (mW)	175.4	4.8	5.4	74.1 (whole chip)

Figure 6. Comparison table of LNA parameters

CONCLUSION

This project demonstrates the design of a single-ended cascode LNA for the Galileo E1 band, implemented in TSMC 65 nm CMOS technology. The final design achieved a simulated noise figure of 0.99 dB and a gain of 19.78 dB, successfully meeting the core performance goals based on recent academic and commercial designs.

To reach this level of performance, the design used a simultaneous noise and power matching strategy along with bias and sizing optimization. This approach resulted in a power consumption higher than typical low-power designs, but it reflects an intentional trade-off to achieve sub-1 dB NF.

Future work may explore low-power design strategies such as reducing the supply voltage, relaxing the NF target, or using alternative topologies and biasing to improve the noise-power trade-off.

Overall, this work offers valuable insight into performance trade-offs and showcases the design potential of custom CMOS RF front-end receivers.

REFERENCES

[1] F. Palhinha et al., "RF Front End Receiver for GPS/Galileo L1/E1," Procedia Technology, vol. 17, pp. 54-62, 2014.

[2] G. Rivela et al., "A 65 nm CMOS Low Power RF Front-End for L1/E1 GPS/Galileo Signals," Great Lakes Symposium on VLSI (GLSVLSI'11), May 2011.

[3] G. Rivela et al., "A Low Power RF Front-End for L1/E1 GPS/Galileo and GLONASS Signals in CMOS 65nm Technology," IEEE Transactions on Circuits and Systems, 2011.